S4PRO

SMART AND SCALABLE SATELLITE HIGH SPEED PROCESSING CHAIN

Interoperable Hardware Solutions & Future Missions

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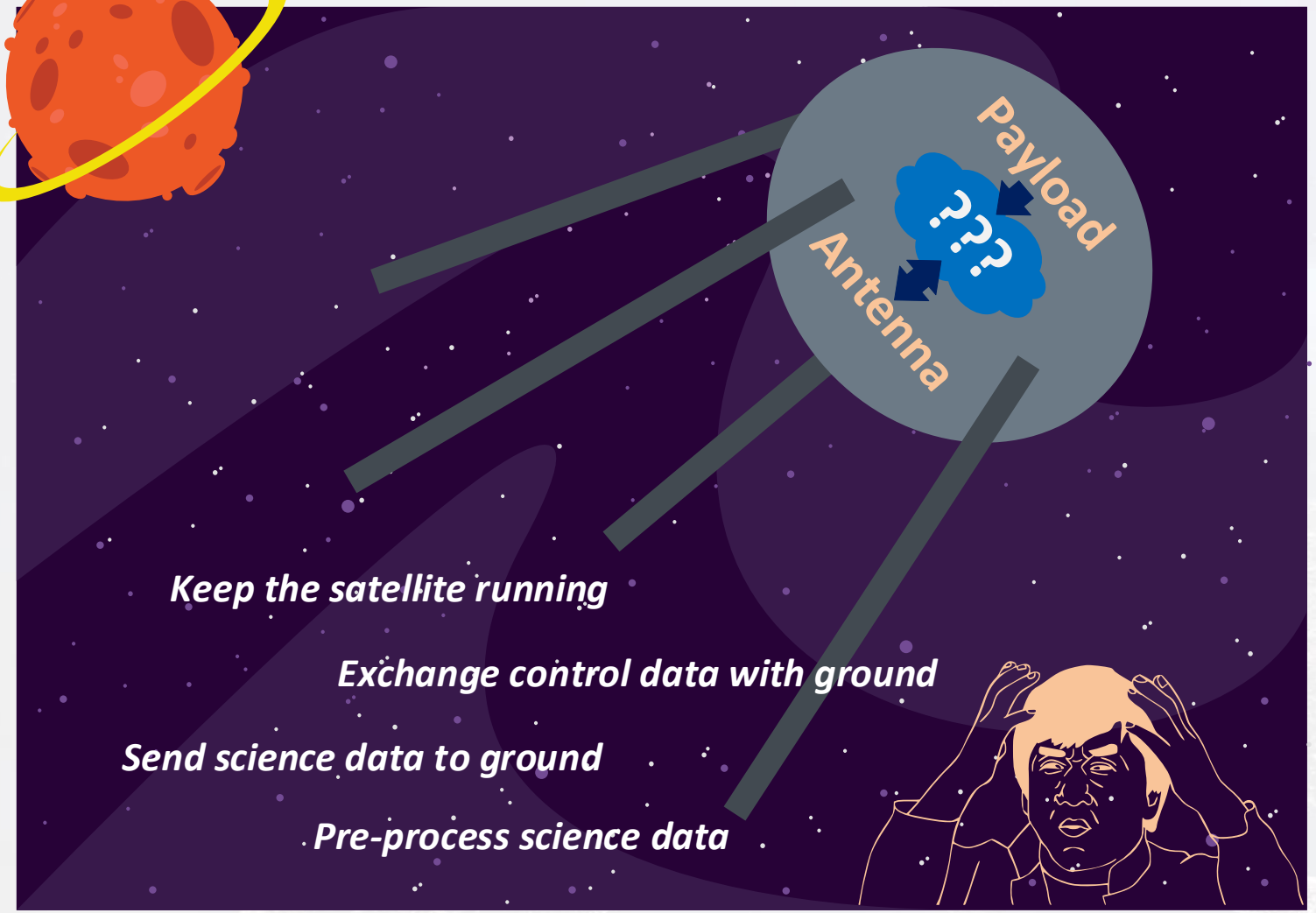
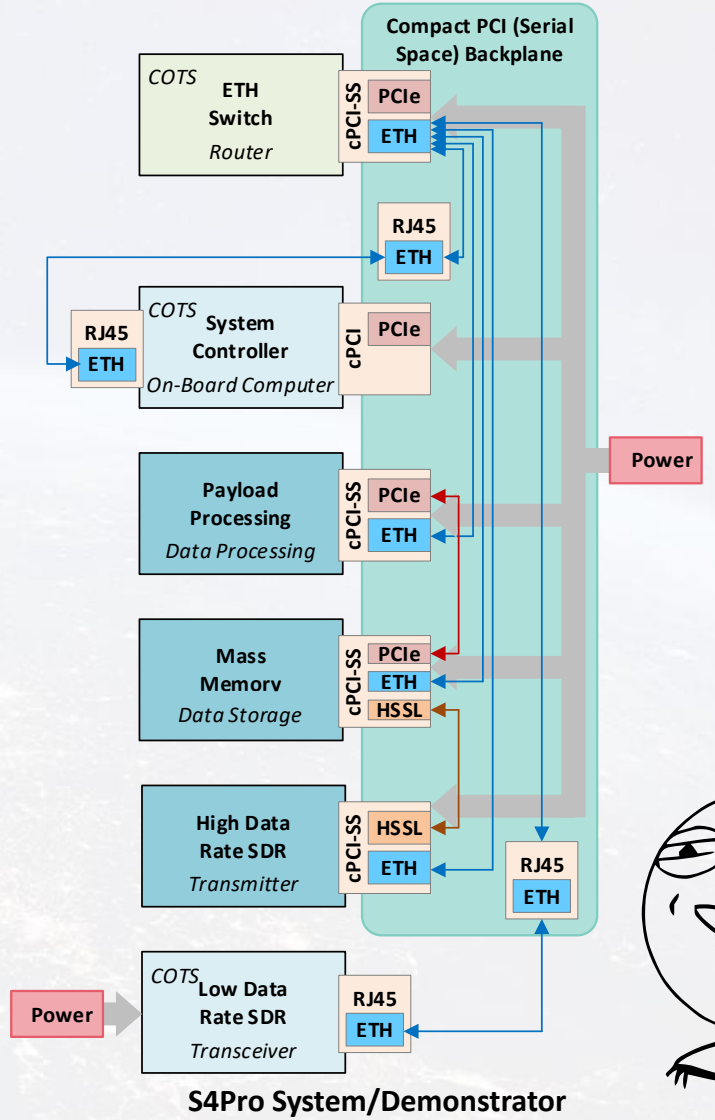
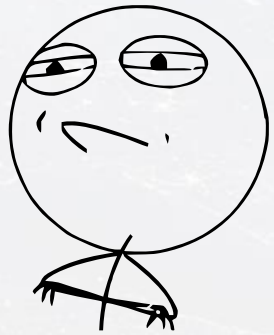
Data Chain of a Satellite





S4Pro System/Demonstrator



USE CASES AND REQUIREMENTS

HW Requirements (sub-set)

- S4Pro modules shall be compliant with the electrical and mechanical interface as defined in **PICMG CPCI-S.1 R1.0**
- The **mass** for an S4Pro board shall be below **500 g**
- The **volume** for an S4Pro module shall not exceed **233.35 mm x 160 mm x 25.4 mm**
- The maximum **power** consumption for an S4Pro module shall be less than **79.8 W** for a **3U** sized module or **171 W** for a **6U** sized module
- The maximum continuous **input data rate** to the mass memory module storage array shall be at least **6 Gbps**
- The mass memory module shall be able to **replay** stored data with a **data rate** of at least **2.5 Gbps**
- The **storage capacity** of the mass memory module shall be at least **4 Tbit** (BOL)
- The **C&C interface** shall be implemented using **Ethernet or SpaceWire** via the cPCI-SS backplane
- The high data rate **transmitter** shall be able to **output** data to the RF front-end with at least **1 Gbps**

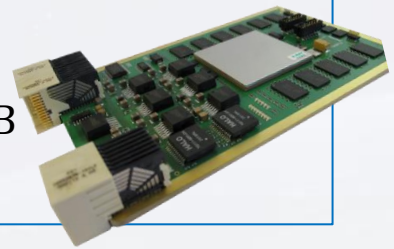
GNSS Requirements (sub-set)

- S4Pro system shall be capable of hosting GNSS receiver board.
- The mass for an SDR module shall be below 750 g
- The SDR Board shall be feed with 9-36V DC power-supply.
- S4Pro system shall include an Ethernet interface to communicate with Navigation & Communication SDR board.
- Navigation & Communication module software/firmware shall be compatible with specific SoM: ADRV9364-Z020/ADRV9361-Z035
- GNSS receiver shall be able to operate in "Ground Snapshot" operating mode.
- GNSS receiver shall be able to operate in "Space Snapshot" operating mode.
- GNSS receiver shall be able to compute PVT using GPS/Galileo Multi-Constellation

SUMMARY OF RESULTS

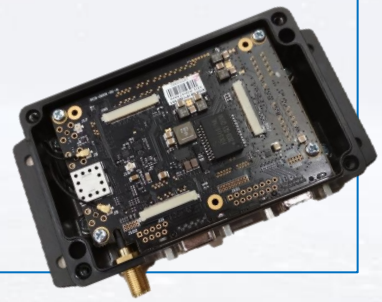
Payload Processing Unit (iTUBS)

- Xilinx Zynq Ultrascale+ EG
- 2x PCI-E 2.0 x8 (up to 32 Gbit/s)
- ECC-protected 8 GB SDRAM
- EDAC-protected 8 GB SDRAMs



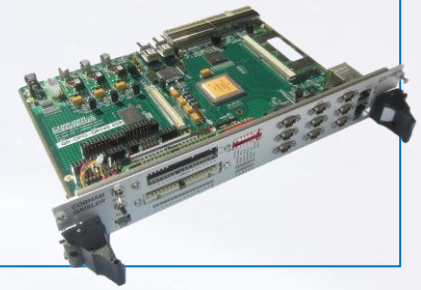
Low Data Rate Transceiver (QAS)

- SDR-based GPS/Galileo receiver
- Snapshot positioning technique to limit power consumption and data-rate
- Position accuracy lower than 12m



COTS System Controller (DSI)

- LEON4 quad-core 32-bit CPU
- PCIe, ETH, MIL-1553, CAN and SpW
- RTEMS OS
- cPCI (6U)

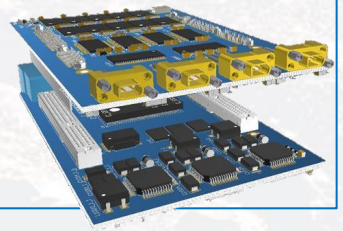


Mass Memory Module (DSI)

- 4 Tbit NAND flash
- 6 Gbps Input via PCIe
- 5.1 Gbps Output via WizardLink
- SpW, PCIe, ETH, WL
- cPCI-SS (6U)
- RTG4 FPGA

High Data Rate Transmitter (DSI)

- 1 Gbps DL via WizardLink
- ASK, PSK, QPSK…
- SpW, PCIe, ETH, WL
- cPCI-SS (6U)
- Kintex Ultrascale FPGA



PAYLOAD PROCESSING – SPECIFICATION AND ARCHITECTURE

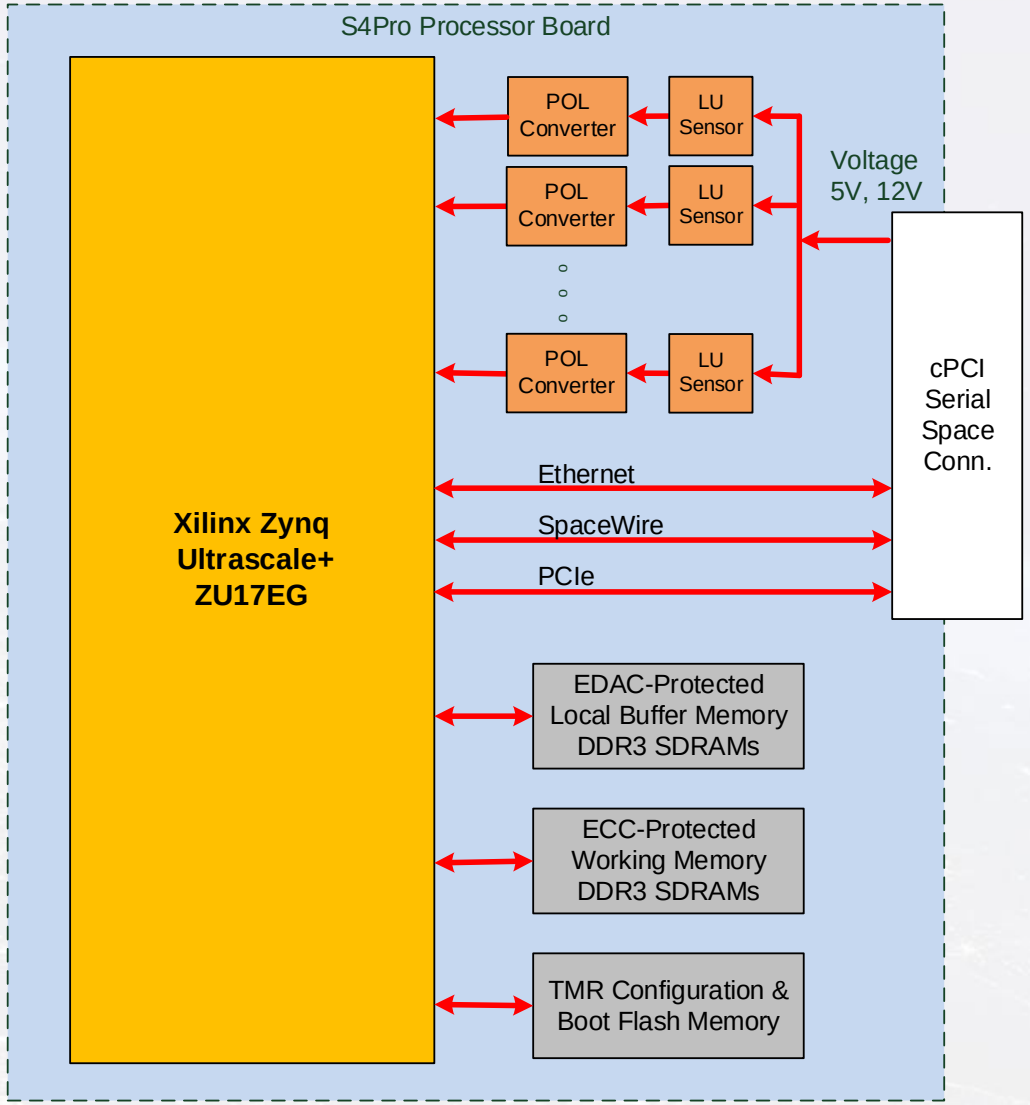
Overview of the S4Pro Navigation & Communication Board

MPSoC: Xilinx Zynq Ultrascale+ EG

- 4 x Arm Cortex-A53: to 1.5 GHz
- 2 x Cortex-R5: to 600 MHz
- Working Memory: ECC-protected 8 GByte SDRAMs
- Local Buffer Memory: EDAC-protected 8 GByte SDRAMs
- Boot-Memory: 256 MByte TMR NOR-Flash

Primary Interfaces

- PCIe 2.0
- Ethernet
- SpaceWire



Payload Processing – Results

Results

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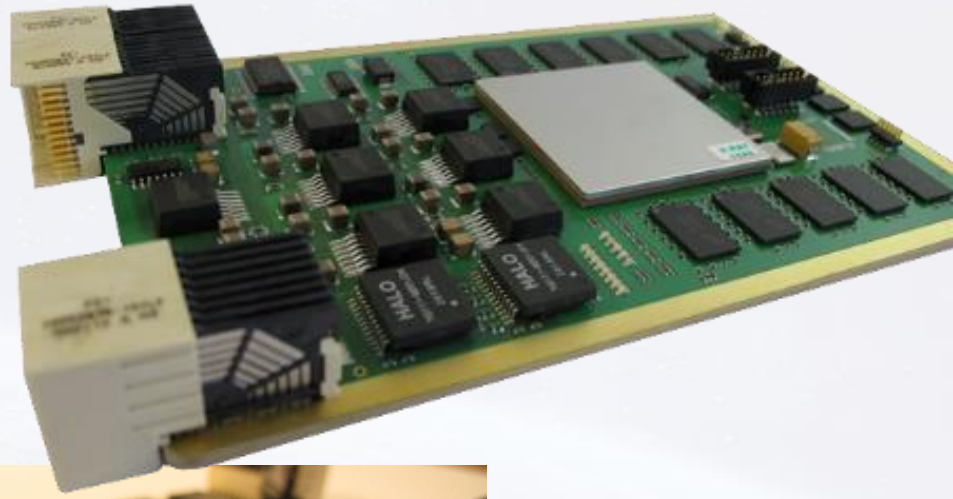
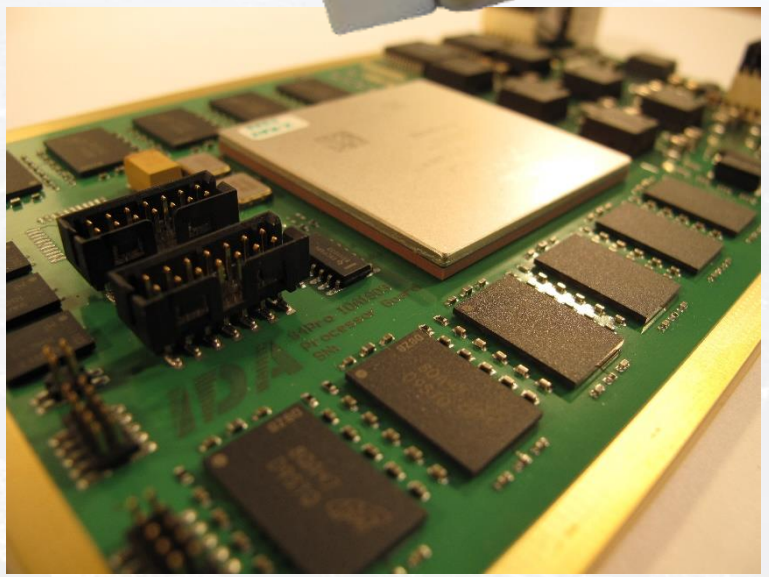
- 2x PCI-E 2.0 x8 (up to 32 Gbit/s)





Low Data Rate Transceiver – Specification and Architecture

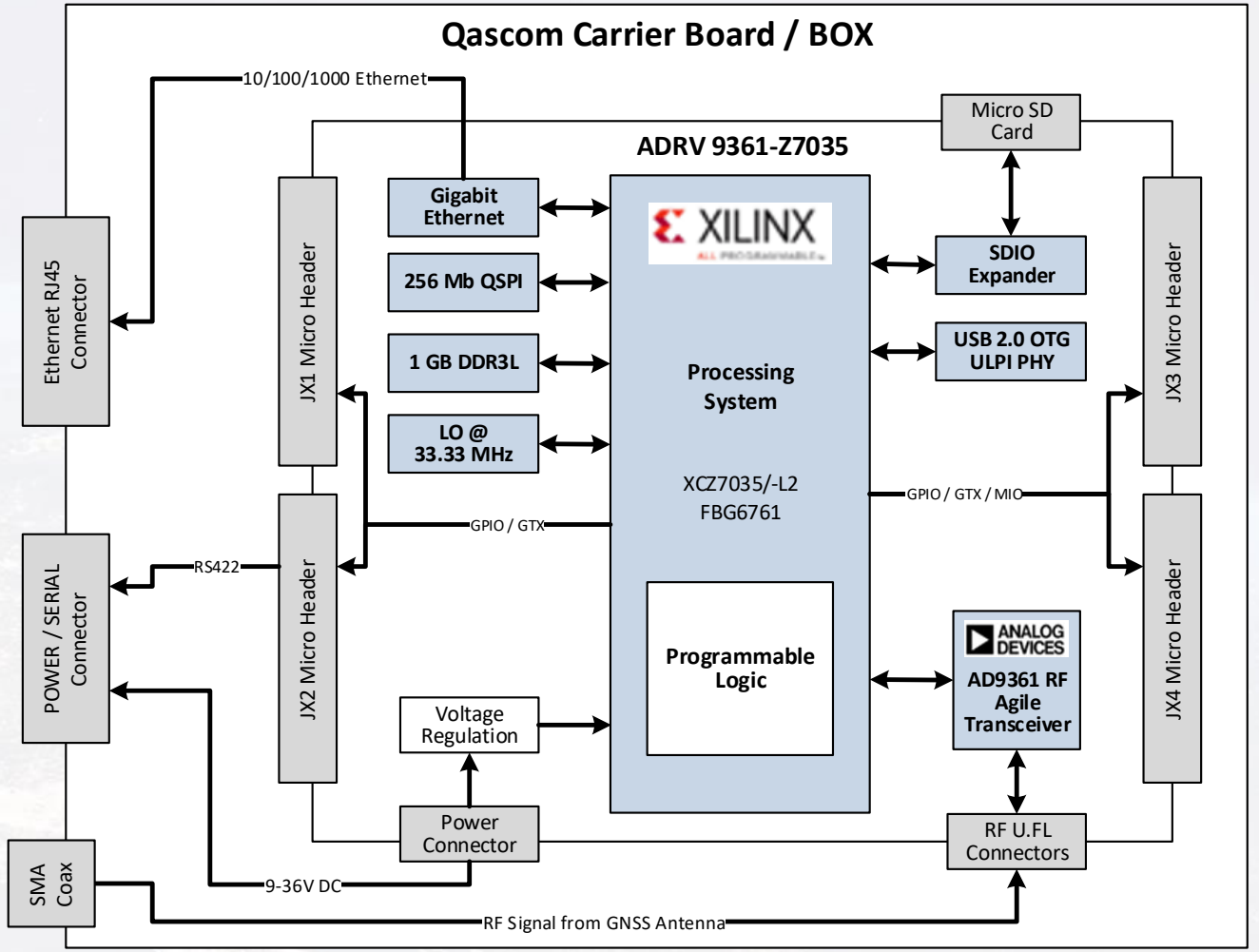
Overview of the S4Pro Navigation & Communication Board

Based on COTS ADRV9361-Z7035 SoM

- RF Frontend: AD9361 (Analog Devices)
- RF Band: 70MHz to 6.0GHz
- Processor: Dual ARM® Cortex™-A9 MPCore™ running at 800MHz
- Programmable Logic: 275K Kintex-7 logic cells with 900 DSP48 slices
- DDR3L: 1GB DDR3L (low power) @ 1,066 Mb/s

Primary Interfaces

- ARM: Gigabit Ethernet, USB2.0, UART, SDI
- User I/O: 209 single-ended or 93 LVDS (up to 1250 or 1400 Mb/s DDR)



Low Data Rate Transceiver – Results

Results

- Radio Frequency ports tested and calibrated in GPS/Galileo L1/E1 band
- Power Supply tests are completed
- Ethernet communication tests performed at 10/100/1000 Mbps using RJ45 and custom D-Sub 15 pin connectors
- Standard hardware interfaces/connectors enables the usage of COTS test equipment (i.e. GNSS Simulators, dataloggers, etc.)
- Software/Firmware functional tests successfully performed
- Performance tests on stability and precision of the GNSS navigation are on-going

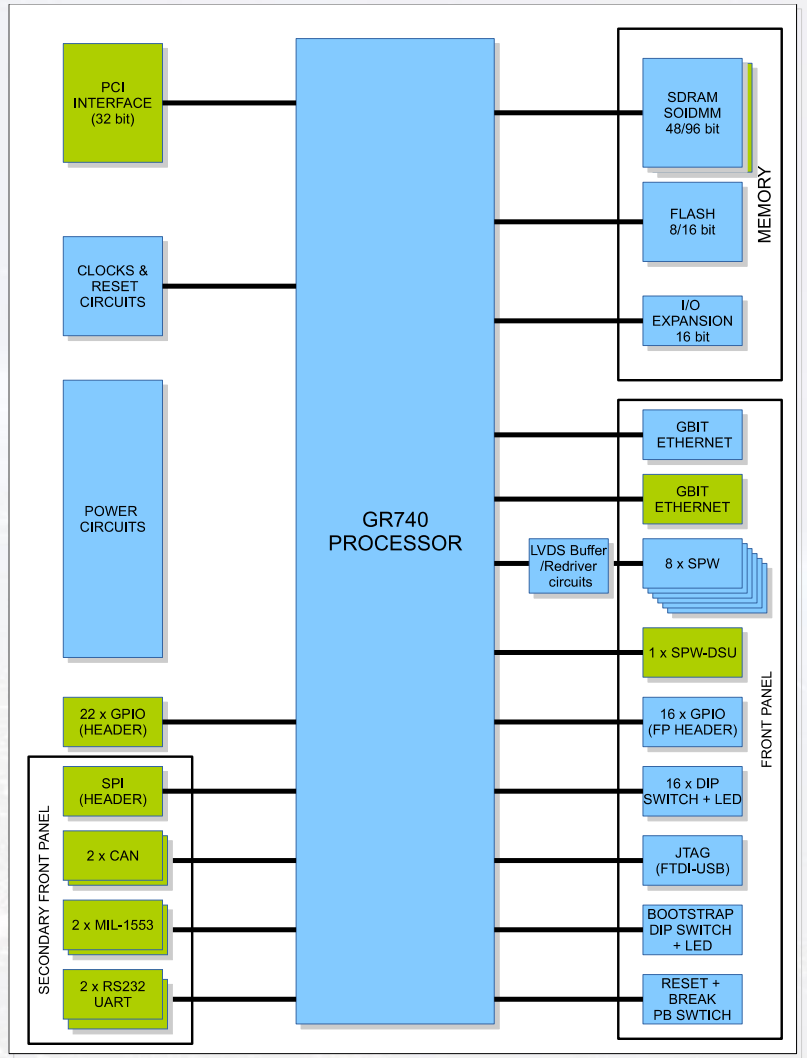
System Controller – Specification and Architecture

Overview

- cPCI electrical and mechanical design
- 6U form factor : 160 mm × 233 mm
- LEON4 quad-core 32-bit SPARC V8 processor
- SDRAM working memory
- Boot flash memory
- RTEMS OS v5

Primary Interfaces

- Data: PCIe
- C&C: Ethernet, CAN, MIL-1553 and SpW



Architecture of the GR740 Dev Board

System Controller – Results

Results

- System controller board integrated in rack
- S4Pro HW demonstrator is a 19’’ rack that can hold multiple 3U and 6U boards
- Interconnections on board level is realized with a backplane
- Multiple break-out adapters form the backplane. Connections between the single boards via cables

S4Pro Demonstrator with 6U GR740 Dev Board

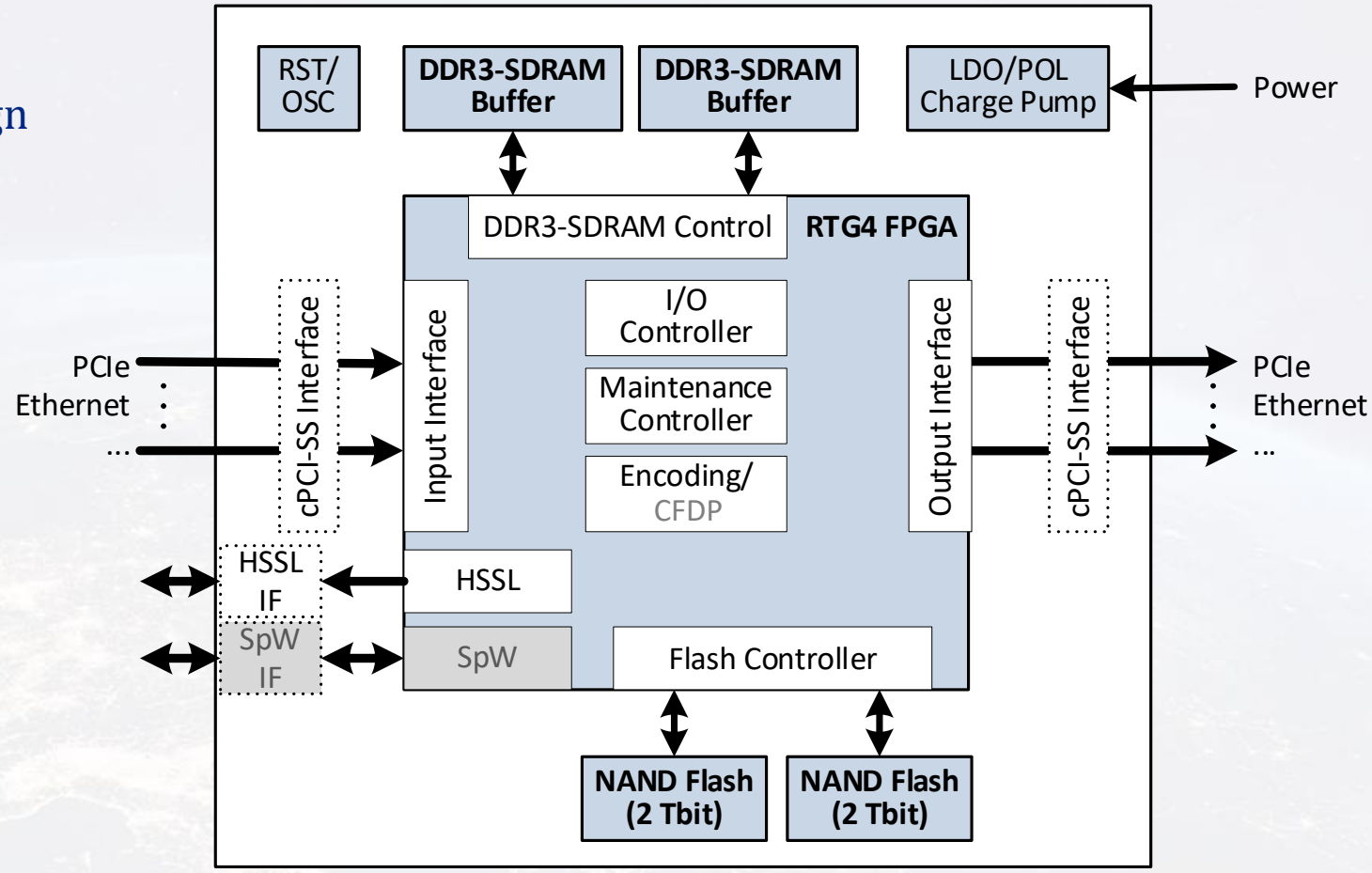
Mass Memory – Specification and Architecture

Overview

- **cPCI-SS** electrical and mechanical design
- **6U** form factor : 160 mm × 233 mm
- **RTG4** based mass memory unit
- **4 Tbit** NAND flash memory
- **DDR3** buffer memory

Primary Interfaces

- Data: **PCIe** and **WizardLink**
- C&C: **Ethernet** and **SpW**

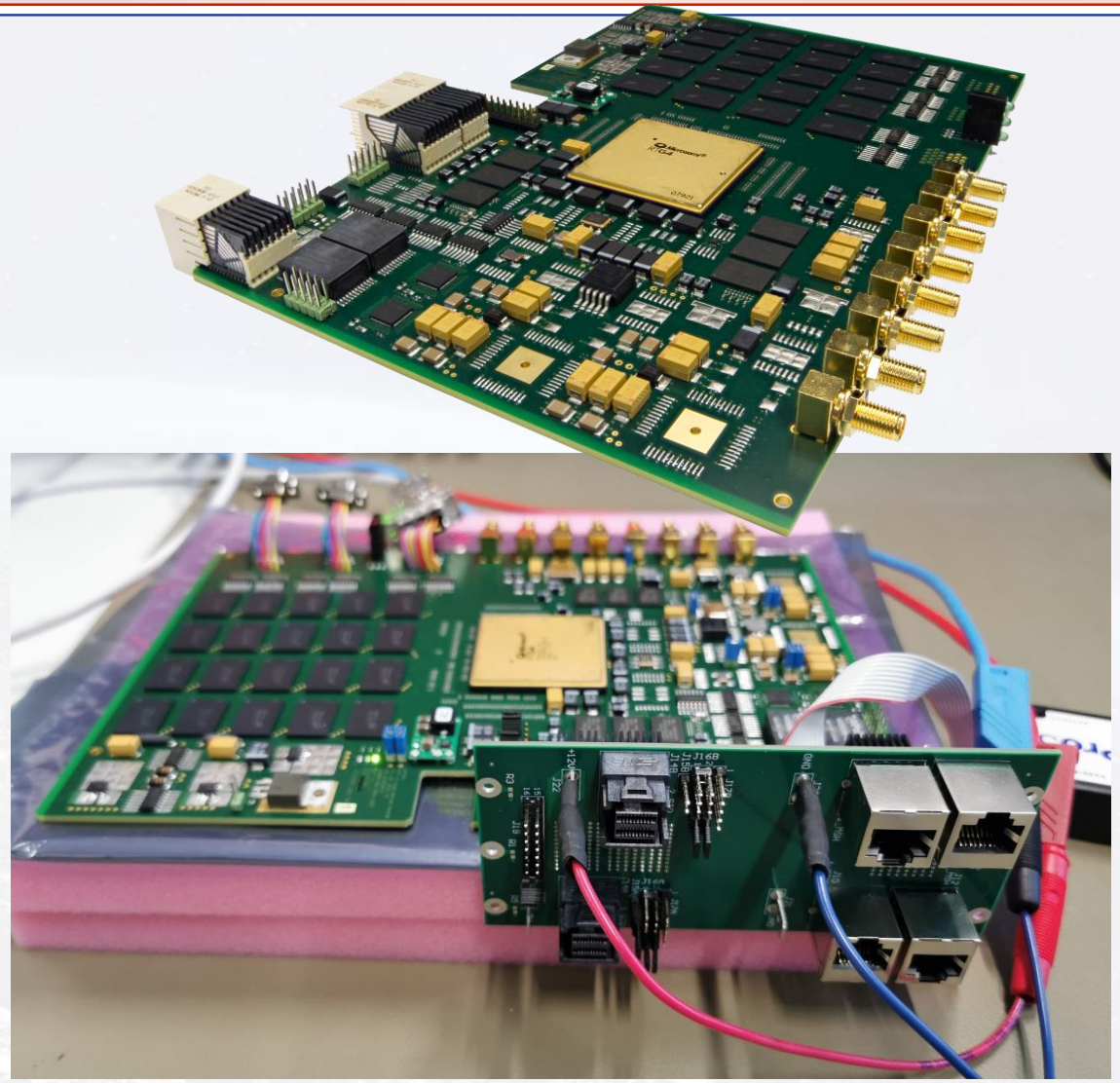


Architecture of the Mass Memory Module

Mass Memory – Results

Results

- Data storage from different independent input interfaces (**up to 6 Gbps** total, customizable)
- Data downlink (**up to 5.1 Gbps**, customizable)
- Simultaneous read/write (max aggregate data rate **5.1-6 Gbps**)
- Power Consumption: < **8W**
- Mass: < **500g**



Mass Memory Module EM with cPCI break-out adapter

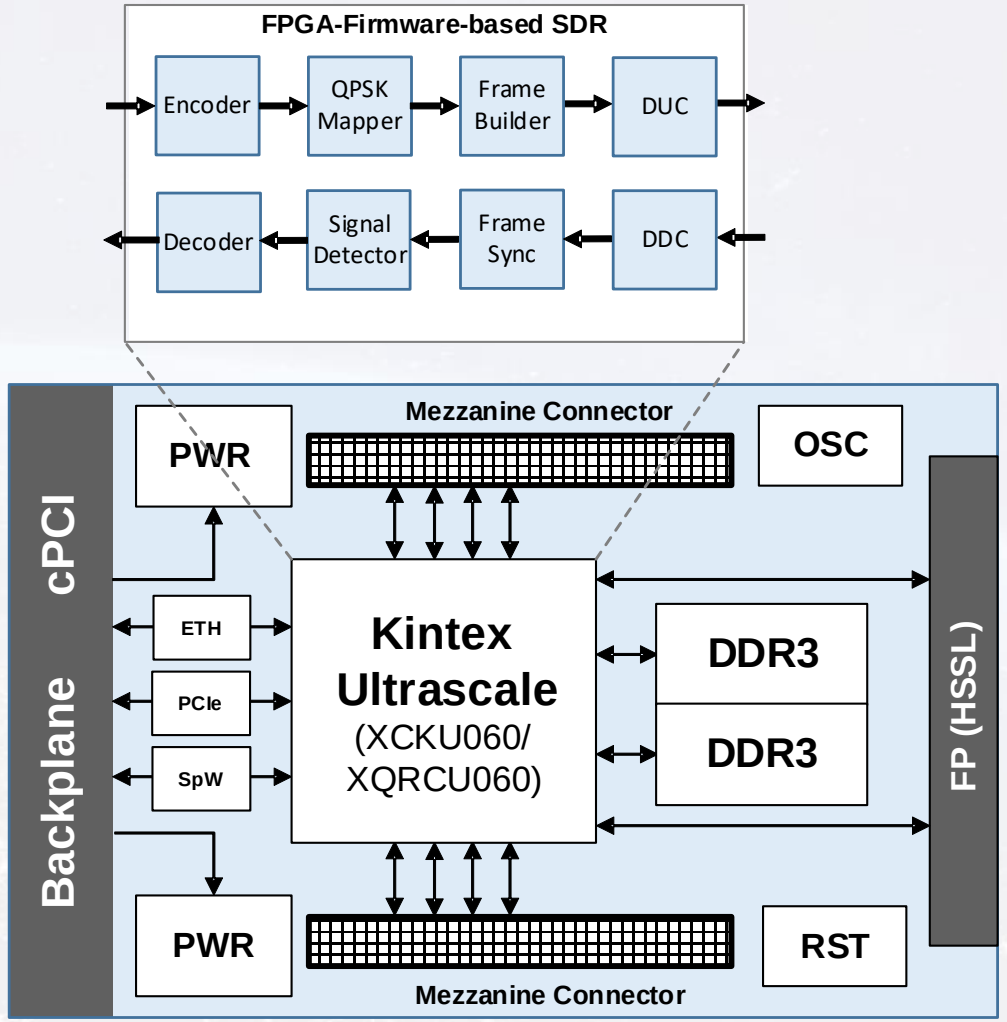
HIGH DATA RATE TRANSMITTER – SPECIFICATION AND ARCHITECTURE

Overview

- Flexible 'working horse' for high performance on-board computing
- cPCI-SS electrical and mechanical design
- 6U form factor : 160 mm × 233 mm
- **1 Gbps** Downlink
- Xilinx Kintex UltraScale FPGA (XQRKU060)
- DDR3 (**8GB**) working memory

Primary Interfaces

- Data: **PCIe** and **WizardLink**
- C&C: **Ethernet** and **SpW**
- Mezzanine connectors (**FMC**) to allow expandability (e.g. Flash partitions, SDR RF Frontends)

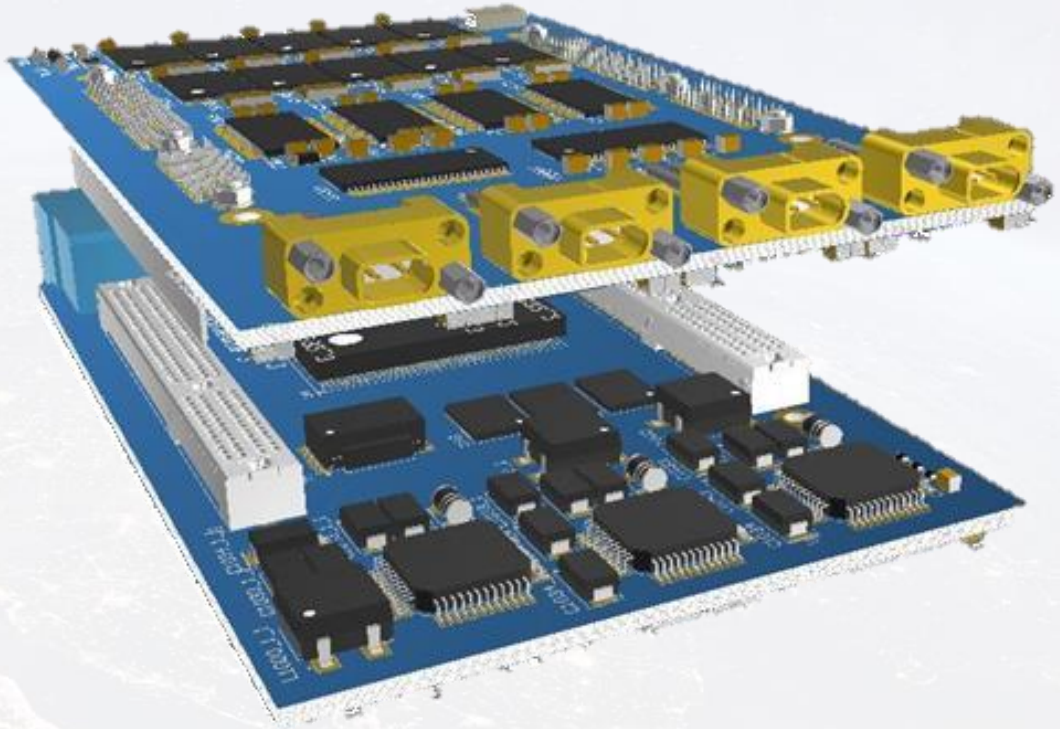


Architecture of the high data rate transmitter

High Data Rate Transmitter – Results

Results

- Full-custom FW FPGA Design
- Reconfigurable during runtime
- Data rate to RF front-end: 1053.44 Gbps
- Supported Modulation: ASK, PSK, QPSK…
- BCH Encoding (0.948)
- Zadoff-Chu Preamble generation for frame sync
- Power consumption: < 15 W
- Mass: < 800g



High data rate transmitter (3D render)

Future Missions

iTUBS

- Time-Triggered Ethernet
- Qualification
- Integration into nanosat
- Using different Processor for the next generation

Qascom

- Real-Time positioning
- Robutness and Interference mitigation
- Multiple frequencies (GPS L1/L5, Galileo E1/E5a)
- Resistance to high dynamics

DSI

- Synchronous flash devices
- ECSS compliant RTG4 fan-out
- CFDP SW/FW implementation
- RISC-V soft-core
- NanoXplore FPGA
- Time-Triggered Ethernet

THANK YOU

ANY QUESTIONS?

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