

D1.4 – On-board Hardware (Storage and Communication) Requirements

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List of acronyms

Acronym/abbreviation	Description
BIT	Build In Test
BOL	Beginning Of Life
CA	Consortium Agreement
C&C	Command & Control
CCSDS	Consultative Committee for Space Data Systems
CFS	Certificate on the Financial Statement
CFDP	CCSDS File Delivery Protocol
CO	Confidential to the Consortium (including EC services) dissemination
cPCI	CompactPCI
cPCI-SS	cPCI Serial Space
DP	Deliverable Process
DoA	Description of Action
EC	European Commission
EU	European Union
GA	Grant Agreement
GNSS	Global Navigation Satellite System
GUI	Graphical User Interface
HW	Hardware
IMR	Internal Management Report
IPR	Intellectual Property Rights
LDO	Low-Dropout
MMM	Mass Memory Module
MS	Milestone (Project)
NAND	NOT-AND
NASA	National Aeronautics and Space Administration
OSC	Oscillator
ORDP	Open Research Data Pilot
PBSOTA	Progress beyond the state of the art
PCI	Peripheral Component Interconnect
PCIe	PCI Express

Acronym/abbreviation	Description
PM	Person Months
POL	Point Of Load
PU	Public (dissemination)
RE	Restricted (dissemination)
REA	Research Executive Agency
RF	Radio Frequency
RST	Reset
S3NET	Satellite Swarm Sensor Network
S4Pro	Smart and Scalable Satellite High-Speed Processing Chain
SAB	S4Pro Advisory Board
SAR	Synthetic Aperture Radar
SDR	Software Defined Radio
SEB	S4Pro Executive Board
SGA	S4Pro General Assembly
SPF	Single Point Failure
SPO	S4Pro Project Office
SW	Software
TBC	To Be Confirmed
TM	Telemetry
TRL	Technology Readiness Level
WBS	Work Breakdown Structure
WP	Work Package
WPL	Work Package Leader

1 EXECUTIVE SUMMARY

This technical requirements document defines the technical requirements for the following hardware modules in the S4Pro project:

- The Mass Memory Module (see Section 3.3)
- The System Controller Module (see Section 3.4)
- The High Data Rate SDR Module (see Section 3.5)
- The Low Data Rate SDR Module (see Section 3.5)

Since some requirements affect multiple modules a section with general HW requirements is introduced (see Section 3.2).

The S4Pro system modules defined in this document will be able to fulfil these requirements and perform all the demands in this document.

2 INTRODUCTION

2.1 Purpose and Scope of Document

This document defines the different communication-related processing requirements and different on-board storage requirements, as derived from the identified subset of applications [AD01], payload processing requirements [AD03] as well as from on-board management software requirements [AD02]. It also derives the relevant S4Pro storage requirements.

2.2 Applicability

This document is applicable to the S4Pro project led by Innovationsgesellschaft Technische Universität Braunschweig mbH (iTUBS) and subcontractors (if applicable).

2.3 Applicable and Reference Documents

2.3.1 Applicable Documents

The following documents form part of this document to the extent specified herein.

Without indication of the issue, they are applicable in their latest issue. In the event of conflict between the contents of this document and the contents of applicable documents as listed below, this conflict shall be brought to the attention of the project management of the involved parties for clarification. Until formal clarification, the particular part of this document remains valid.

Doc. Ref.	Document No.	Document Title, Issue/Date, Organization
AD0	D1.1	S4PRO Applications and Mission Scenarios, OHB-I
AD0	D1.2	On-board Management Software Requirements, iTUBS
AD0	D1.3	On- Board Payload Processing Requirements, DLR

Table 1 : Applicable Documents

2.3.2 Reference Documents

The documents listed below were used in the preparation of this document and contain additional information.

Without indication of the issue, they are applicable in their latest issue. In the event of conflict between the contents of this document and the contents of reference documents as listed below, this conflict shall be brought to the attention of the project management of the involved parties for clarification.

Doc. Ref.	Document No.	Document Title, Issue/Date, Organization
RD01	PICMG® CPCI-S.1 R1.0	cPCI Serial Space™ Specification
RD02	PICMG® CPCI-S.0 R2.0	CompactPCI® Serial Specification

Table 2 : Reference Documents

3 HARDWARE REQUIREMENTS

3.1 Hardware Overview

The S4Pro system hardware is architected around the cPCI Serial Space standard, with each module connected to a cPCI-SS backplane for inter-module communication. This backplane routes power and data between each S4Pro module, with secondary power provision performed on each module individually.

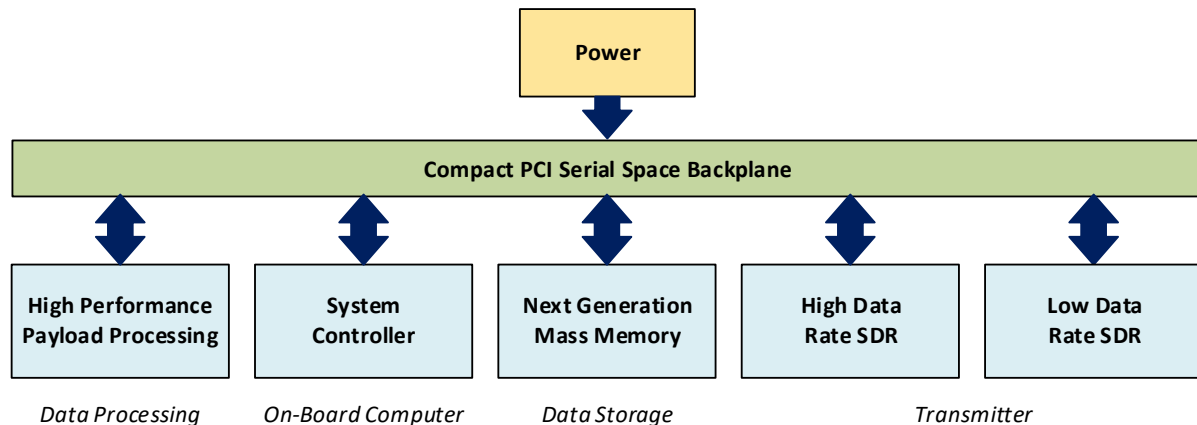


Figure 3-1 : S4Pro cPCI-SS Architecture¹

Each S4Pro system module will be designed to accommodate PCIe and Ethernet communication over the cPCI-SS backplane, along with the 12 V main power bus and 5 V standby power bus. The power bus in the S4Pro project is not required to originate in a cPCI card, but may be delivered from an external power supply.

3.1.1 S4Pro HW Objectives

The S4Pro hardware is designed to provide a path to achieving the payload processing and storage requirements for future high performance missions, including those described out in D1.3 [AD03].

3.1.2 S4Pro HW Architecture

The S4Pro system is designed around using the cPCI-SS standard to deliver a flexible solution for payload processing, on-board computing, data storage, and downlink subsystems. The cPCI-SS standard provides a capable electrical and mechanical interface definition that will allow multiple hardware vendors to collaborate on a single mission while reducing design risk around the critical interfaces. In addition, the architecture will accommodate the high performance systems needed for future missions with high data throughput and storage requirements. It will also be scalable, able to accommodate mission large and small with minimal changes to the hardware design.

Each S4Pro system module will have a primary cPCI-SS interface containing the power and data interfaces to the rest of the S4Pro system. A very high-level diagram can be seen in Figure 3-2.

¹ Please note that the requirements of the payload processing module are not part of this document

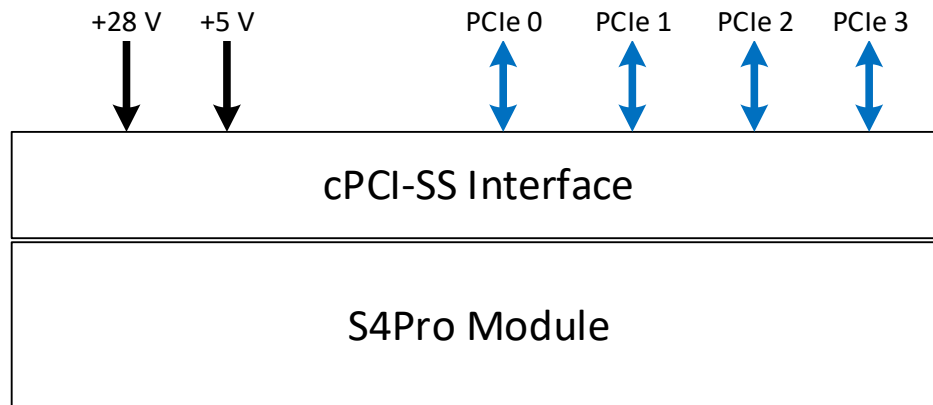


Figure 3-2: S4Pro cPCI interface

The S4Pro system will contain several cPCI-SS modules to form a single system capable of handling the functionality including on-board processing, data storage, data processing, and data downlink. The nominal design includes no single-point-of-failure by installing redundant modules. The cPCI-SS interconnect standard provides redundant connections between modules.

In Figure 3-3, the MMM is shown with its primary cPCI-SS interface, along with the internal structure of the system. The MMM interface to the rest of the system via the cPCI-SS interface and internally contains all the components and interfaces necessary to fulfil its functional requirements.

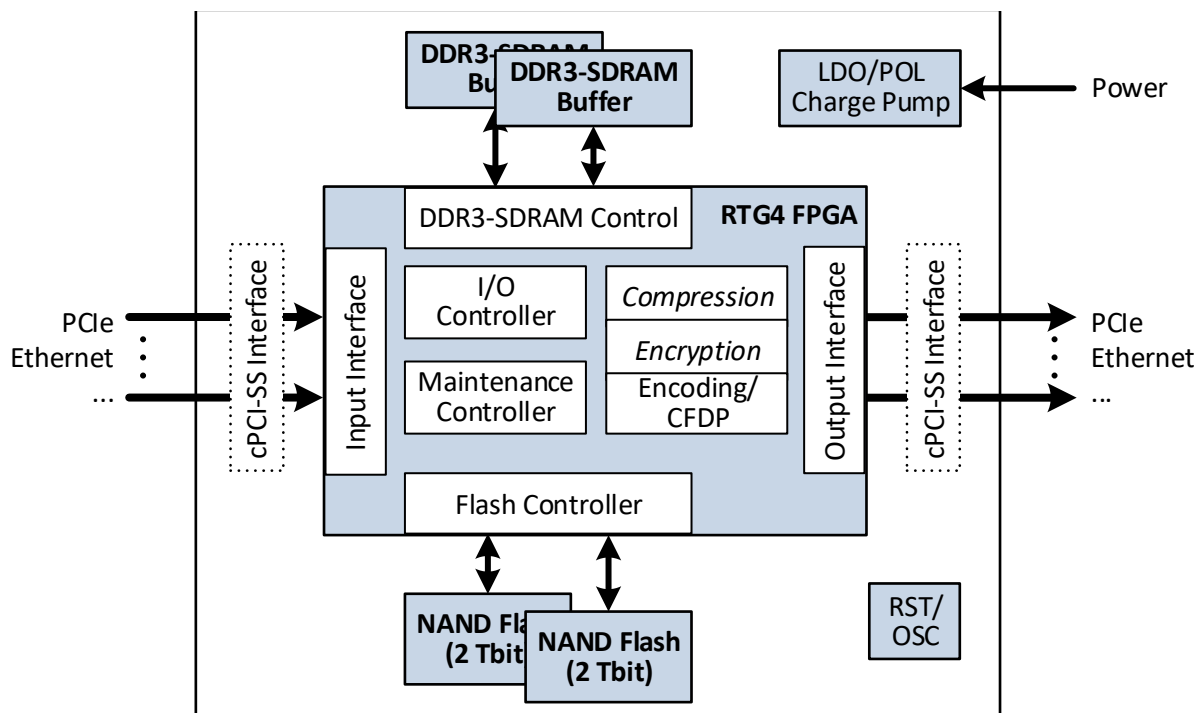


Figure 3-3: MMM Block Diagram²

The system controller for use in S4Pro will be the GR-CPCI-GR740 Development Board. This will interface to the cPCI-SS bus, provide all the command, and control functions for the S4Pro system.

² Compression and encryption won't be part of S4Pro, but could be implemented in a future design with the same HW

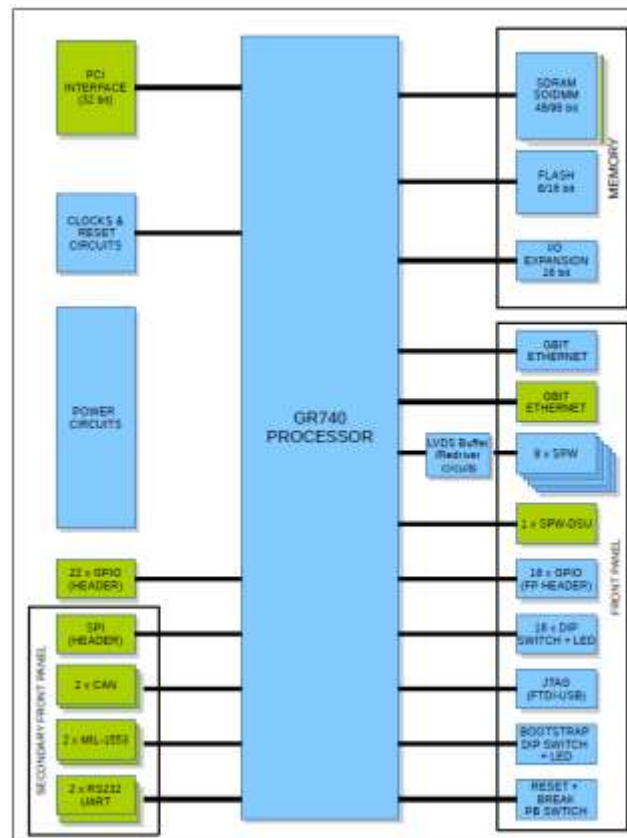


Figure 3-4: GR-CPCI-GR740 Development Board Block Diagram

The System controller module is based on an off-the-shelf module. Thus, the hardware requirements are limited to the module itself and all functional requirements must be met in the configuration of the development board and in software.

3.2 General HW Interface Requirements

3.2.1.1 General Electrical Interface

S4Pro HW modules shall be compliant with the electrical interface as defined in RD01 and RD02.

3.2.1.2 General Mechanical Interface

S4Pro HW modules shall be compliant with the mechanical interface as defined in RD01 and RD02.

3.2.1.3 Mass

The mass for an S4Pro module shall be in accordance with 3.2.1.2.

3.2.1.4 Volume

The volume for an S4Pro module shall be in accordance with 3.2.1.2.

3.2.1.5 Power Consumption

The maximum power consumption for an S4Pro module shall be less than 79.8 W for a 3U sized module or 171 W for a 6U sized module [TBC].

3.2.1.6 Power Interface

The power interface shall be compliant with the mechanical interface as defined in RD01 and RD02.

3.2.1.7 Lifetime

The unit shall be designed for a nominal operational lifetime of 7 years, following a commissioning period of up to 6 months.

3.2.1.8 Element SPF

An individual S4Pro module is not required to be single point failure free.

3.3 Mass Memory Module HW Requirements

3.3.1.1 Functionalities

The following functions shall be present in the MMM:

- Reception and storage into the mass memory of data, packet store
- File based operation
- CFDP
- Time based file operations
- Deletion of stored files
- Telemetry encoding
- Output of stored and formatted data
- Simultaneous recording and playback
- Monitoring and control of MMM
- Secondary power provision for the MMM
- Single point failure-free design

3.3.1.2 Operational Mode: Power Up

This mode is for initiating the MMM. This mode shall manage timing and all needed operations for initiating the system after the power the system.

3.3.1.3 Operational Mode: BIT

In the "BIT" (Build In Test) mode the MMM shall manage timing and work flow for initiating the BIT procedures.

The "BIT" mode will check and verify that the MMM functions right

The results should be available to the user throw the "GUI & Display" mode.

The BIT mode shall start from the Idle mode only, and by the user request only.

3.3.1.4 Operational Mode: Verification

In the "Verification" mode, the MMM shall verify the correctness of the data and intermediate files. The files that will be verified are the files received from the Payload Processing Module.

3.3.1.5 Operational Mode: Nominal

In the "Nominal" mode, the MMM reads, writes, and erases files from the Payload Processing Module to be sent to the Communication module.

3.3.1.6 Operational Mode: Idle

In the "Idle" mode, the MMM is powered on and able to switch modes, but is not currently active.

3.3.1.7 Data Acquisition Rate

The maximum continuous input data rate to the MMM storage array shall be at least 6 [TBC] Gbps.

3.3.1.8 Data Playback Rate

The MMM shall be able to replay stored data through cPCI-SS interface to other system modules with a data rate of at least 2.5 [TBC] Gbps.

3.3.1.9 OBC HK Acquisition Rate

The MMM shall be capable of acquiring HK data from the OBC simultaneously with any other nominal operation at a data rate of at least 10 [TBC] Mbps.

3.3.1.10 Data Acquisition Interface

The data acquisition interface for input to the MMM storage array from other system modules shall through Ethernet or SpaceWire via the cPCI-SS interface.

3.3.1.11 Data Downlink Interface

The data downlink interface shall be implemented using PCIe or Ethernet via the cPCI-SS backplane over the cPCI-SS interface [TBC] to any data downlink modules.

3.3.1.12 C&C Interface

The C&C interface shall be implemented using Ethernet or SpaceWire via the cPCI-SS backplane.

3.3.1.13 Discreet C&C interface

The MMM shall support a discreet redundant (N+R) C&C interface over SpW.

3.3.1.14 Maximum Storage Capacity

The storage capacity of the MMM shall be at least 4 Tbit (BOL) [TBC].

3.3.1.15 Minimum Storage Capacity

The smallest configuration of storage capacity of the MMM shall be no less than 1 Tbit (BOL) [TBC].

3.3.1.16 Storage Modularity

The storage of the MMM shall be modular to allow for variable storage capacities up to the maximum capacity per 3.3.1.14.

3.3.1.17 Mass

The mass shall be in accordance with 3.2.1.3.

3.3.1.18 Volume

The mass shall be in accordance with 3.2.1.4.

3.4 System Controller HW Requirements

3.4.1.1 General Design

The system controller shall be implemented using a Cobham Gaisler GR-CPCI-GR740 LEON4 development board. All interfaces and specifications are to be defined via the development board user manual GR-CPCI-GR740-UM.

3.4.1.2 Functionalities

The system controller shall perform the following system functions

- TM collection for S4Pro system modules
- Command and Control of S4pro system modules
- Mass Memory Flash Array file system management

3.4.1.3 Communication Interface Compatibility

The system controller shall be able to communicate with the other S4Pro modules via the cPCI backplane interface

3.4.1.4 Processing Functionality

The system controller shall be capable of processing any required commands to the rest of the S4Pro modules in real time.

3.5 Communication HW Requirements

3.5.1 Communication System Functionalities

3.5.1.1 Downlink

The communication system shall provide a transmitter capable of outputting data to a RF front end for downlink.

3.5.1.2 High Speed Downlink

The communication system shall provide a high speed downlink output for an X-Band based radio system.

3.5.1.3 High Speed Downlink Input Interface

The high speed downlink input interface shall use Ethernet or SpaceWire via the cPCI-SS interface

3.5.1.4 Low Speed Downlink

The communication system shall provide a low speed downlink output.

3.5.2 Navigation and Communication SDR

S4PRO Navigation and Communication processing capabilities will be performed on a single board, by leveraging SDR technology in space. A single module with GNSS Receiver, and integrated Telemetry (TM) signal, will demonstrate the capability in space to geo-tag EO data. The demonstration that GNSS data can be combined with EO data will extend the current known capability of GNSS for precise EO data location acquisition determination.

3.5.2.1 Space Processing Layer Architecture

The Space Processing Layer Software will run on an SDR COTS board composed by:

- **State of Art System on Chip:** ADRV9361-Z7035 That represent the state of the Art of the Digital Signal Processing. These devices that are built on a portfolio of highly integrated System-On-Module (SOMs) based on the Xilinx Zynq®-7000 All Programmable (AP)SoC. Built on the Analog Devices AD9361 and the Xilinx XC7Z035-L2FBG676I, it is schematically & HDL similar to the AD-FMCOMMS3-EBZ.

Some of the features and specifications of the module are listed below:

Fully-verified, low-power, rugged system-on-module (SOM) ready for end-product deployment

- Industrial temperature rated, production-ready SOM
- Conforms to MIL-STD 202G for thermal, vibration, and shock
- Included on SOM:
 - Analog Devices AD9361-BBCZ Integrated RF Agile Transceiver™
 - Xilinx Zynq XC7Z035-2L FBG676I AP SoC
- Software tunable across wide frequency range (70MHz to 6GHz)
- Less than 200kHz to 56MHz channel bandwidth
- Supports MIMO radio, with less than 1 sample sync on both ADC and DAC

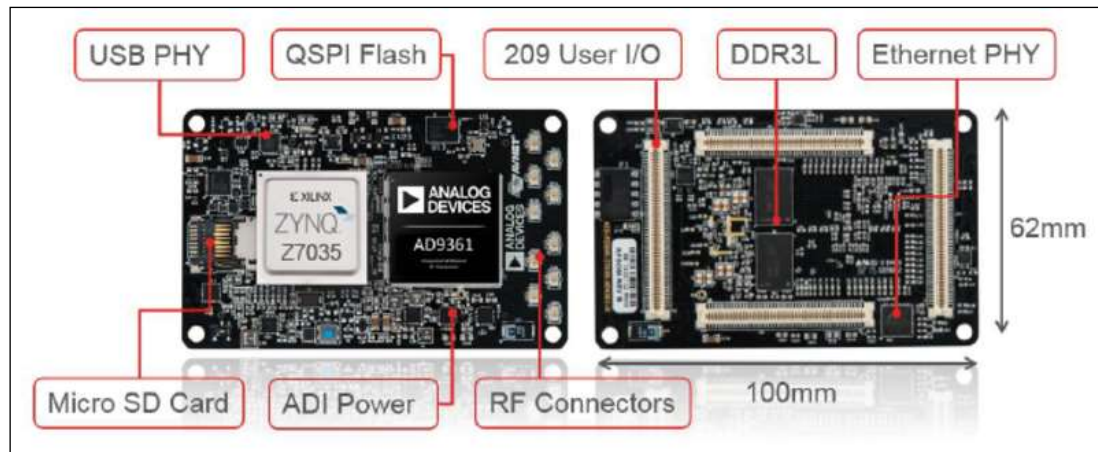


Figure 3-5: ADRV9361-Z7035 SoM

- **ADRV1CRR-BOB Breakout Carrier:** a platform for the SDR 1x1 and 2x2 SOMs, providing easy access to user I/O, Ethernet, USB, JTAG, and serial connections.

Four 100-pin Micro Headers on the carrier card mate with the SDR SOM, connecting the user I/O to 6 banks of 0.1" through-hole connector footprints. The Breakout Carrier generates the necessary power rails for the SDR SOM, providing 5V to the SOM plus user selectable bank voltages for the Xilinx Zynq Programmable Logic I/O. In addition, the carrier provides multiple access points to supply external I/O bank voltages and measure power consumption of the SOM.

- **Feature List**
 - 10/100/1000 Mbps Ethernet
 - USB2.0 OTG
 - USB-UART
 - PC4 JTAG interface
 - 162 User I/O pins
 - Two 60-pin (2×30) 0.1" footprints
 - Four 32-pin (2×16) 0.1" footprints
 - user push buttons
 - user switches
 - user LEDs
 - 5V @ 2A input
 - Select 1.8V, 2.5V, or 3.3V for SOM I/O or insert an external supply
 - Measure Zynq PL I/O bank current with convenient access points

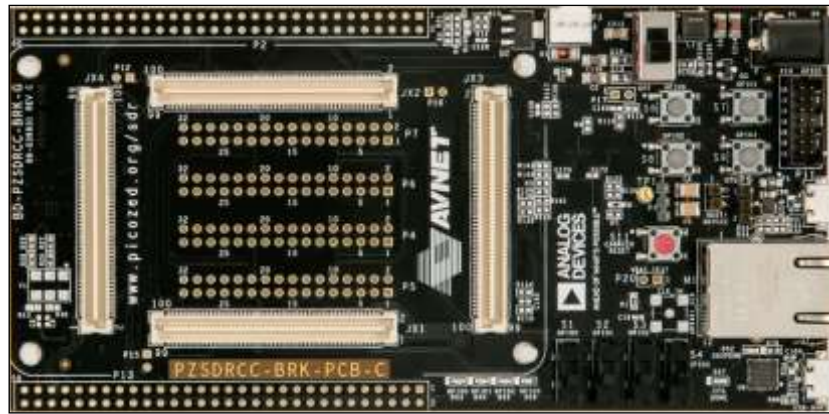


Figure 3-6: ADRV1CRR-BOB Breakout Carrier

3.5.1 Physical Interfaces

The ADRV9361 module already connected to its carrier (ADRV1CRR-BOB), has an RJ45 socket to host an Ethernet cable. The Ethernet Physical and Data Link layers will consist of the network interfaces of the ADRV9361 and the on-board-computer hosting the Management Software. At Network layer, IP protocol will be used in order to permit TCP/IP (Transport layer) connections between the applications.

In the end, between GNSS SoM and Management Software a **TCP/IP** connection will be established. In both operational modes data will be transferred through the on-board Ethernet interface, as shown in Figure 3-7.

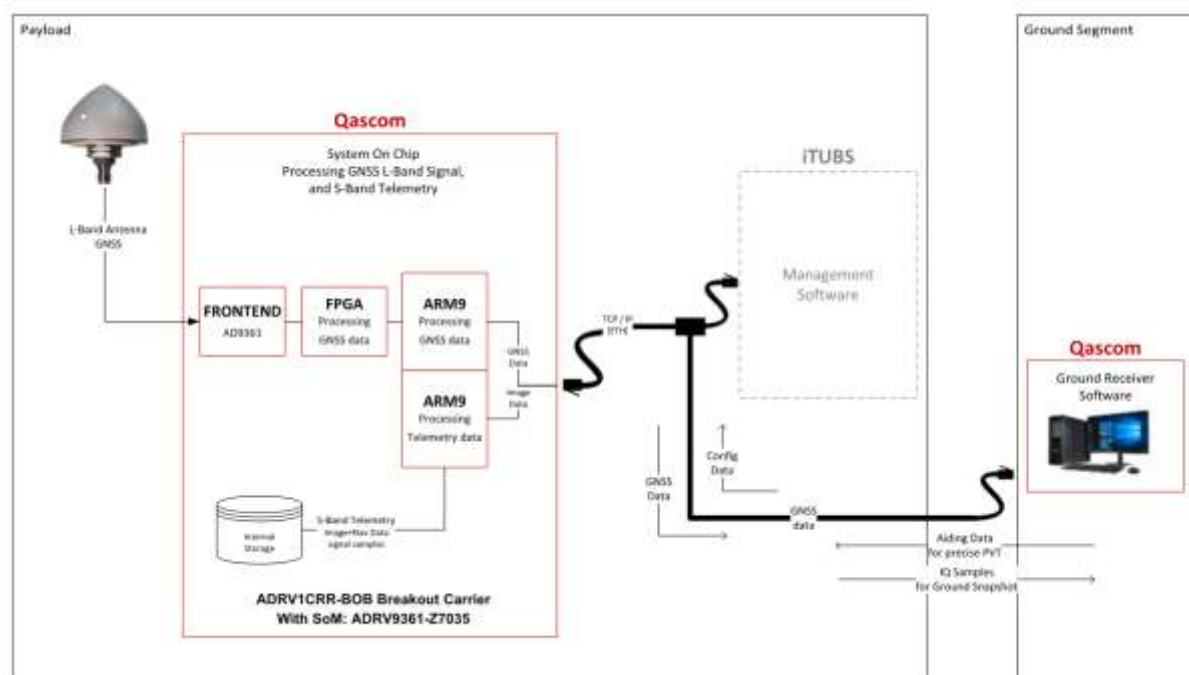


Figure 3-7: Space Architecture

The ADRV9361 is the TCP server, its network adapter will have a static IP address, and one or more ports (that will be refined during next phases of the project) through which a set of permanent connections will be established, for different type of data exchanges.

3.5.2 On Board L-Band processing

A snapshot is a short recording of the raw data after digitalization of the IF signal in the front-end (short recording means that it is in the order of seconds or milliseconds). Snapshot processing is a kind of A-GPS in the sense that it also requires data from external sources. However, it does not work in a continuous manner and often positioning is computed in post-processing.

S4PRO GNSS application processing chain is based on RF signal coming from the on-board L-Band Antenna.

3.5.2.1 IQ Snapshot Acquisition

The first step to get a signal snapshot, consist in converting the analog signal into digital IQ samples. This and further signal processing techniques, are performed by the FPGA, in order to improve performances.

Those signal samples are stored locally for the short amount of time necessary to compute the processing that is a series of techniques aimed to permit the resolution of PVT equation system using only few milliseconds of signal.

3.5.2.2 GNSS SNAPSHOT processing PVT

The snapshot processing approach foresees the sampling of a GNSS signal batch and the application of several signal processing techniques to compute the PVT solution.

The Space Processing Layer will support two different processing modes:

- Space Snapshot Processing (SPACE-SNP)
- Ground Snapshot Processing (GROUND-SNP)

For each of the processing mode a specific Software Architecture will be implemented. The software will be developed with a high level of modularity, reusing the FPGA and Software components for the two processing modes that are described in the following:

Space Snapshot Processing (SPACE-SNP): The snapshot processing approach foresees the sampling of a GNSS signal batch and the application of several signal processing techniques to compute the PVT solution. The logical architecture of the Snapshot Processing operation mode includes:

1. **Sample SW:** it is a Middleware (driver) implementing the interface between the RFFE ADC and the FPGA, including quantization of the signal.
2. **FPGA FW:** including the
 - i acquisition engine based on FFT (dedicated to Snapshot Processing)
 - ii Noise Floor Estimation Channel
 - iii Clock / Timing Management
3. **MID SW:** Middleware implementing the interface between the FPGA and the microprocessor
4. **Microprocessor Software:** including the:
 - i Receiver manager
 - ii Acquisition Logic
 - iii Measurements Generation
 - iv Message Decoding
 - v Other processing

5. **Applications** that are the different plugins that can be installed in the receiver.
6. **Communication module:** it is responsible for transmitting and receiving information to/from Management Software and Ground PC, through the ethernet connection. It receives configuration data and transmits back the data produced by the receiver.

Ground Snapshot Processing (GROUND-SNP): in the operation mode GROUND-SNP the samples collected with the satellite RF frontend are provided to ground, where the processing is achieved. In the space segment the SDR board retrieves the signal sampled by the frontend and provides it to the Ground Segment. The logical architecture of the space processing layer that shall support Ground Snapshot Processing operation mode includes a limited number of functional blocks, specialized for the transmission of samples on ground:

1. **Sample SW:** it is a Middleware (driver) implementing the interface between the RFFE ADC and the FPGA, including quantization of the signal.
2. **TC/TM IF interface module:** it is responsible for transmitting and receiving information to/from ground, through the provided transceiver. It receives configuration data and transmits back the data produced by the receiver.

3.5.2.3 Tx over ETH of IQ or PVT

In Ground snapshot Processing (GROUND-SNP), the samples collected with the satellite RF frontend are provided to ground, where the processing is achieved. In the space segment the SDR board retrieves the signal sampled by the frontend and provides it to the emulated TC/TM link (Ethernet connection). The logical architecture of the space processing layer that shall support Ground Snapshot Processing operation mode includes a limited number of functional blocks, specialized for the transmission of samples on ground:

1. **Sample SW:** it is a Middleware (driver) implementing the interface between the RFFE ADC and the FPGA, including quantization of the signal.
2. **Communication module:** it is responsible for transmitting and receiving information to/from ground, through the transceiver. It receives configuration data and transmits back the data produced by the receiver.

3.5.2.4 Processing of aiding data from ground

In Space Snapshot processing (SPACE-SNP) the receiver acquires and processes the signal in space with a snapshot approach, using aiding data transmitted from the ground. This allows the spacecraft to achieve the navigation in space with lower energy consumption, because snapshot approach is not continuous and performs less operations with respect to a Real-Time Processing approach.

Aiding information such as GNSS satellites ephemeris and receiver TLE, allows the receiver to precompute a rough estimation of the GNSS signal dynamics to reduce Doppler frequency search space and therefore reduce the acquisition time and computational load. The algorithm uses aiding information to reduce the search window: ephemerides, receiver coarse position and kinematic state of the spacecraft are required to perform navigation solution.

3.5.2.5 Geo/Time-Tagging of EO data

SPACE-SNP and GROUND-SNP approaches show a main difference in terms of data payload to transfer. While ground snapshot requires much more data (raw IQ samples) to be transferred, space snapshot will dramatically reduce the amount of data.

Just to give an example: 100 milliseconds of signal snapshot, at a sampling rate of 5MHz, each IQ sample represented with 16-bit integer, will lead to roughly 2Mb of data to be transferred to ground. While injecting directly a computed PVT in an image, is a matter of typically less than 100 bytes (51 bytes for the simplest example below).

45.4500030,N,011.4400057,E,2019-02-11T23:59:59.900Z

The pro of GROUND-SNP technique is that almost all computational effort can be demanded to ground PC, leaving to the on board SoM only the task of saving the snapshot. While SPACE-SNP pros resides mainly on the reduced amount of data to be merged with EO data, at the expense of power consumption.

3.5.3 On Board S-Band processing

3.5.3.1 Retrieval data from Optical subsystem

EO data to be geo/time-tagged and transmitted as Telemetry flows from the Management Software to the GNSS module. ARM microprocessor application inside Navigation & Communication hardware board merge incoming EO data with Navigation Data, and then apply data coding and modulation to get Telemetry (TM) signal samples raw data, ready to be transmitted.

3.5.3.2 TM data modulation packet

The Standard mode modulation formats (as per [RD.1]) shall be Phase Modulation (PM) on Telemetry downlink. The standard mode for Telemetry is known as MTM1, generated by a sine wave sub carrier, itself BPSK modulated by PCM data.

Reference signal generation provides message generation, an Upsampling module for setting the symbol stream to the sampling frequency or to the code rate, a PCM encoding block, and finally the PSK/PM.

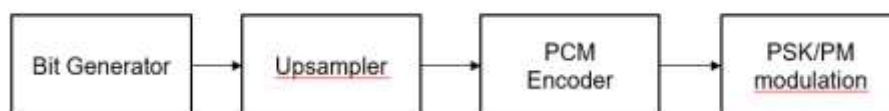


Figure 3-8: Chain from bit generation to PSK/PM Modulation

Where, in detail the PCM/BPSK/PM modulation scheme is shown in Figure 3-9.

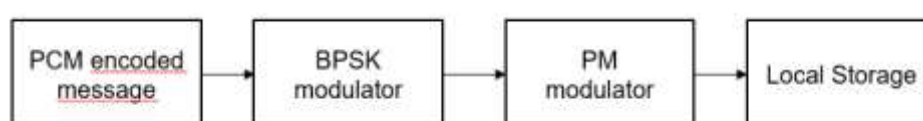


Figure 3-9: Chain from PCM Message to Local Storage

3.5.3.2.1 Upsampler

Upsampling is necessary in order to have the reference signal at desired sampling rate. In particular the function accomplishes a square wave upsampling. If d is the output sequence and b the original one, the output vector is defined by:

$$d(n) = b \left[\text{floor} \left(\frac{n-1}{f_s/S_r} \right) + 1 \right] \quad (1)$$

Where f_s is the sampling frequency and S_r the reference signal symbol rate (indexing starts from 1, as in Matlab notation).

3.5.3.2.2 PCM encoding

The upsampled message has to be PCM encoded before being processed by Baseband modulation block. Standards under test require basically three kinds of encoding modes that may be set accordingly to documents [RD.1], [RD.2] and [RD.4]:

- NRZ-L
- SP-L
- NRZ-M

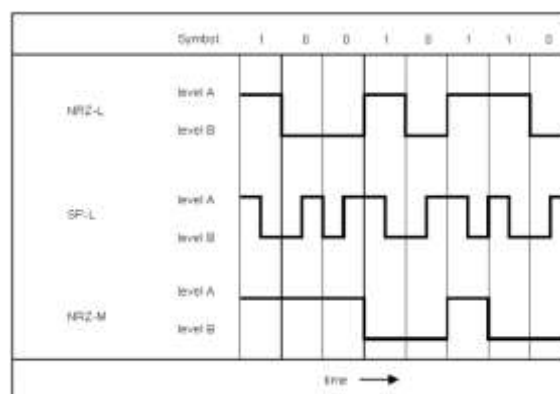


Figure 3-10: PCM Encoding

Setting level $A = 1$ and level $B = -1$, NRZ-L assigns 1 to elements ones and -1 to the zeros.

SP-L sets first half symbol 1 and second half symbol -1 for bits one and vice versa for zeros.

In NRZ-M, a symbol change corresponds to 1 and constant symbol corresponds to 0.

3.5.3.2.3 PCM/BPSK/PM Baseband modulation

PCM/BPSK/PM signal modulation (as per [RD.2]) is accomplished by two blocks (ref. to Figure 3-11):

BPSK modulator, PM modulator.

BPSK modulator block multiplies the reference bit stream with a sinusoid of frequency equal to the chosen sub-carrier f_{sc} , the output signal then modulates the main carrier by means of a PM modulator block and generates PCM/BPSK/PM signal. The final generator output is given by:

$$s(t) = \sqrt{2P} \cdot \sin(2\pi f_0 t + m \cdot d(t) \cdot \sin(2\pi f_{sc} t + \theta_{sc})) \quad (2)$$

Where m is the modulation index, $d(t)$ the input symbol at t instant, f_{sc} the sub carrier frequency (0,1 kHz to 1000kHz for MTM1), θ_{sc} the sub carrier phase, f_0 the carrier frequency and P the transmitted power.

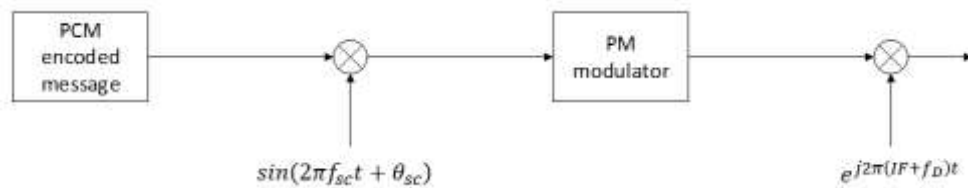


Figure 3-11: PCM/PSK/PM baseband modulation scheme

An example of real Telemetry Signal spectrogram is shown in figure... using sub-carrier frequency = 20kHz, symbol rate = 10ksym/s, and sampling frequency of 1MHz.

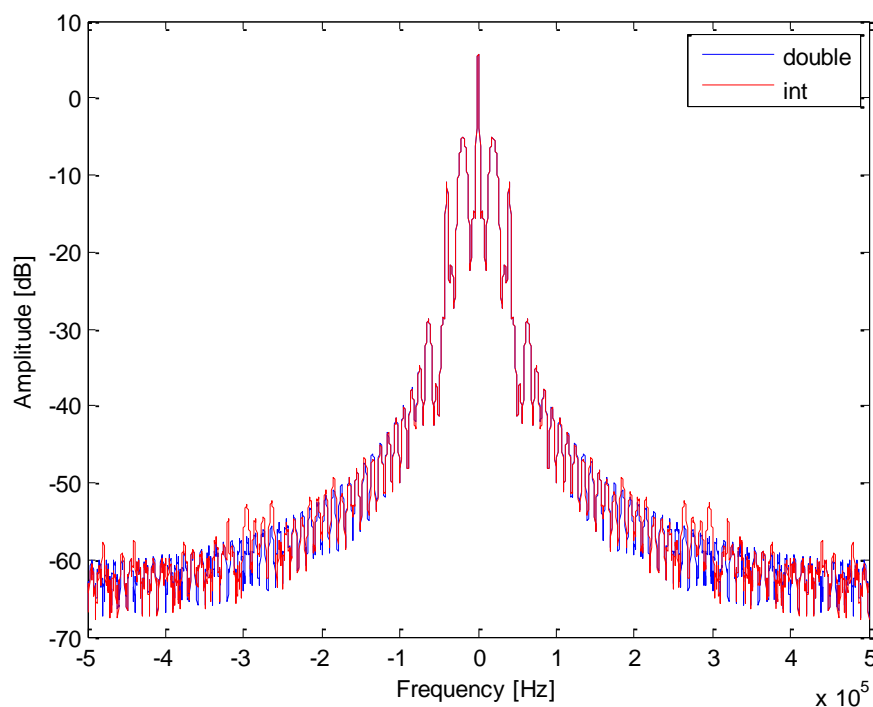


Figure 3-12: Welch plot for Telemetry sample signal

As shown in the figure above, most of the signal power will be transmitted in 200 kHz, so using a sampling frequency of 1Msps, is more than enough to reconstruct the signal.

3.5.3.3 Telemetry Signal Data Storage

Telemetry Signal samples are saved in RAW binary format, interleaved-IQ, in the local storage.

Supposing to save each I and Q sample component as an int16 (16-bit integer value), the disk usage for each second of signal is roughly $10^6 * (2_{IQ} * 2_{bytes}) = 40Mb$.

Software-driven data storage for raw IQ signal, ensure a purging strategy to avoid filling of local storage space.

3.5.4 Hardware Requirements

In Table 3, Table 4 and Table 5 are listed all the hardware requirements for Navigation & Communication SDR Board, accompanied by a brief description.

3.5.4.1 System Level Interface Requirements

Title	Description
SDR module power supply	The SDR Board shall be feed with 5V DC Power-Supply.
GNSS RF signal interface	The system shall include an RF signal interface in the space segment.
Ground segment User Interface	The system shall include a user interface for the ground segment, in order to monitor the system outputs and insert configuration.
Data processing tools interface	The system shall include an interface for the processing of the telemetry data.
SDR module local storage	SDR Board shall include et least 4Gb local storage for raw IQ data (GNSS + Telemetry signals)

Table 3 : System Level Interface Requirements

3.5.4.2 System Level Data Interfaces

Title	Description
Ground segment Data interface	The system shall include an Ethernet interface between the board and the Ground segment for the transmission of aiding information, configuration and signal sample batches.
Management Software Data interface	The system shall include an Ethernet interface between the board and the Management software for the reception of EO data.

Table 4 : System Level Data Interfaces Requirements

3.5.4.3 Hardware Interface

Title	Description
L-Band antenna to SDR module interface	The interface between L-Band antenna and SDR Board shall be a SMA coaxial cable.
L-Band antenna to SDR module signal	The interface between L-Band antenna and SDR Board shall carry the RF GNSS signal.
SDR module to Ground Segment interface	SDR Board and Ground Segment shall be physically connected by Ethernet cable.
SDR module to Management Software cable	SDR Board and Management Software shall be physically connected by Ethernet cable.
SDR module to Ground Segment data rate	The interface between SDR Board and Ground Segment shall have a data rate which is at most 1 Mbps.
SDR module to Ground Segment signal transmission	The interface between SDR Board and Ground Segment shall be bidirectional.

Table 5 : Hardware Interface requirements

3.6 System Environmental Requirements

3.6.1 Thermal Requirements

3.6.1.1 Component Temperature Limits

The qualification temperature limits shall be defined as the following range:

Parameter	Description	Temperature (° C)
T _{Q-OP min}	Qualification Min Temperature	-35
T _{Q-OP max}	Qualification Max Temperature	70
T _{A-OP min}	Acceptance Min Temperature	-25
T _{A-OP max}	Acceptance Max Temperature	60
T _{SU min}	Start-Up Min Temperature	-45
T _{SU max}	Start-Up Max Temperature	80
T _{NO min}	Non-Operational Min Temperature	-45
T _{NO max}	Non-Operational Max Temperature	80

4 CONCLUSIONS

The S4Pro system will comprise advanced space qualified hardware in a cPCI-SS compatible module. The design goal of these modules will be interoperability and to be used in conjunction with other cPCI-SS avionics systems. The high performance of the S4Pro hardware will enable future missions including the target mission parameters given by ROSE-L.

5 BIBLIOGRAPHY

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